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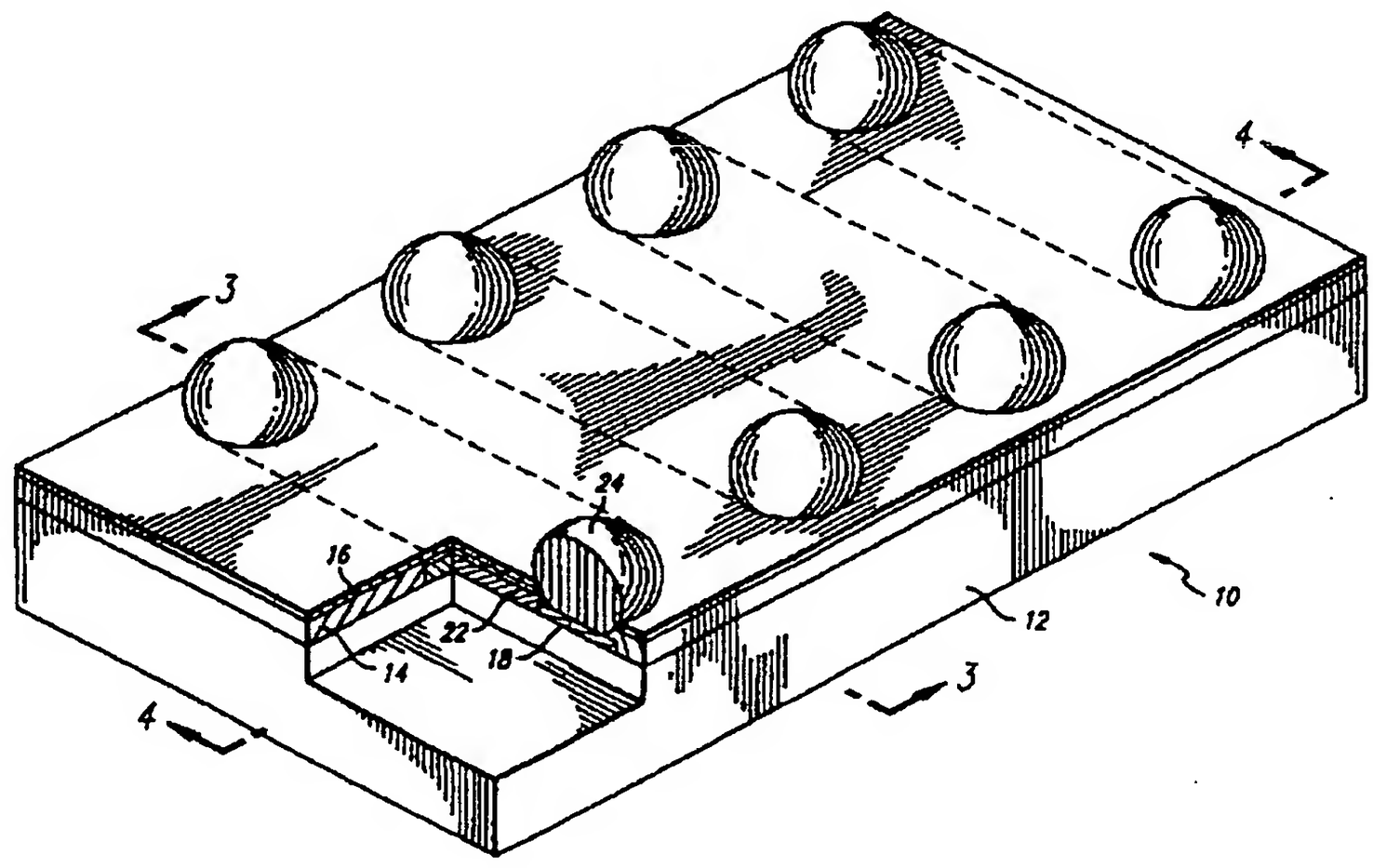

(57) Abstract

A resistor network is provided with a BGA package. The resistor network comprises a substrate (12) having a plurality of electrically conductive pads (18) provided thereon with resistive material disposed on the substrate interconnecting selected ones of the conductive terminals to provide isolated or networked resistors. A protective layer (16) covers the resistive material and the substrate, and a plurality of solder balls (24) are respectively coupled to the plurality of conductive pads. The solder balls enable electrical connection to associated lands of a printed circuit board.

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RESISTOR NETWORK IN BALL GRID ARRAY PACKAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to resistor networks, and more particularly, to a resistor network adapted for ball grid array packaging.

2. Description of Related Art

Resistors are electronic devices that oppose current flow without causing any phase shift to a propagating electrical signal. Traditionally, resistors were individually packaged using axial electrical leads that permit the resistor to be electrically connected to other circuit elements, such as to a printed circuit board. In the last several years, however, it has become increasingly common to include multiple resistors within a single package. In such packages, referred to as resistor networks, the resistors may either be isolated from each other or internally connected together or to a common terminal pin. Examples of common resistor network packaging include single in-line packages (SIP) and dual in-line packages (DIP) used for through-hole or socket mounting onto a printed circuit board, or flat-pack and leadless chip configurations used for surface mounting onto a printed circuit board. Resistor networks enable manufacturers to minimize space and routing problems, reduce manufacturing cost per installed resistive function, and increase circuit board yields and reliability by reducing component counts.

Recently, ball grid array (BGA) packaging has been introduced as an alternative for certain types of integrated circuits. Integrated circuits often have high numbers of leads that are relatively difficult to seat properly into an associated socket. As a result, some of the individual leads may fail to connect to the printed circuit board, or

electrical shorts may be formed between adjacent leads. These problems may be difficult to detect during the manufacturing process, and can result in damage to the integrated circuit or other components of the printed circuit board.

A BGA package overcomes these problems by coupling the circuit to a printed circuit board through solder balls rather than through conventional leads. The solder balls can be arranged in an array or grid pattern so as to increase the density and total number of electrical connections that are formed between an integrated circuit and a printed circuit board. Each solder ball readily self-aligns to an associated land disposed on the printed circuit board. The solder balls then form a conductive bond with the associated lands by use of conventional solder reflowing techniques. The material content of the solder balls can be selected to control their melting rate so that a sufficient gap remains between the BGA device and the surface of the circuit board following the solder reflow process. Alternatively, a permanent bond may be formed through compression of the BGA package against the printed circuit board.

An additional benefit of the BGA packaging is that the solder balls provide good thermal transfer between the BGA device and the circuit board. Moreover, the solder balls provide excellent thermal compliance between the substrate of the integrated circuit and the printed circuit board, thereby minimizing thermal mismatch and improving thermal cycle life. Finally, the solder balls enable a sufficient gap to remain between the BGA device and the printed circuit board enabling cleaning of the printed circuit board following assembly.

Despite these clear advantages of BGA packaging to integrated circuits, a single package that combines the desirable attributes of resistor networks with BGA packaging has been heretofore unavailable. Accordingly, it would be advantageous to provide a resistor network specifically adapted for BGA packaging in order to obtain the benefits of

increased density and improved thermal capacity that have been previously experienced with integrated circuits.

SUMMARY OF THE INVENTION

In accordance with the teachings of the present invention, a resistor network is provided within a BGA package. The resistor network comprises a substrate having a plurality of electrically conductive pads provided thereon with resistive material disposed on the substrate interconnecting selected ones of the conductive terminals to provide isolated or networked resistors. A protective layer covers the resistive material and the substrate, and a plurality of solder balls are respectively coupled to the plurality of conductive pads. The solder balls provide electrical connection to associated lands disposed on a printed circuit board.

More particularly, the resistive material is disposed on a common surface of the substrate as the solder balls, and the solder balls may be disposed in an array pattern. The protective layer further comprises a glaze layer covering the resistive material, and an epoxy layer covering the glaze layer. The resistive material may interconnect pairs of the conductive pads to provide isolated resistors, or may interconnect with a common one of the conductive pads. The substrate may be comprised of aluminum oxide, and the resistive material may be comprised of silver, palladium, platinum, ruthenium, rhodium or gold.

A more complete understanding of the resistor network in a ball grid array package will be afforded to those skilled in the art, as well as a realization of additional advantages and objects thereof, by a consideration of the following detailed description of the preferred embodiment. Reference will be made to the appended sheets of drawings which will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional end view of a prior art resistor network in a leadless chip configuration;

Fig. 2 is a perspective view of a resistor network in a BGA package of the present invention;

Fig. 3 is a sectional end view of the resistor network, as taken through the section 3-3 of Fig. 2; and

Fig. 4 is a sectional side view of the resistor network, as taken through the section 4-4 of Fig. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention satisfies the need for a single package that combines the desirable attributes of resistor networks with BGA packaging. In the detailed description that follows, it should be appreciated that like element numerals are used to describe like elements in one or more of the figures.

Referring first to Fig. 1, a prior art chip resistor array 30 is illustrated. The resistor array 30 is known as a leadless device because it does not have wire leads that would engage a hole or socket of a printed circuit board. Instead, the resistor array 30 attaches directly to the surface of a printed circuit board. Such leadless resistor arrays 30 have a generally low profile, and thus minimize the overall height of a component-filled printed circuit board.

The resistor array 30 comprises a substrate 32 of a thermally conductive, electrically insulative material, such as ceramic. A pair of electrical conductors 34 are provided on opposing side edges of the substrate 32. The conductors 34 wrap around the side edges of the substrate 32 to effectively join an upper surface and a lower surface of the substrate together. At the upper surface of the substrate 32, a resistive element 38 is provided that couples the opposing pair of the conductors 34 at the upper portion thereof. A glaze layer 42 is provided over the resistive element 38 which

additionally covers a portion of the conductors 34. Also, an epoxy layer 44 is disposed over the glaze layer 42 in order to further seal and protect the resistive element 38 following laser trim of the resistive element. The conductors 34 may be additionally coated with a solder layer 36 to facilitate attachment of the resistor network 30 to a printed circuit board.

The resistor network 30 attaches to a printed circuit board at the respective lower surfaces of the conductors 34. Heating of the conductors 34 using conventional solder flow or wave soldering techniques causes the solder layer 36 at the lower surfaces of the conductors 34 to flow into and permanently bond with associated lands disposed on the printed circuit board. It should be apparent with the thickness of the respective conductors 34 defines the spacing between the lower surface of the substrate 32 and the printed circuit board. Thus, it should be apparent that the lower surface of the substrate 32 between the conductors 34 is essentially unusable.

Referring now to Figs. 2 through 4, a resistor network 10 constructed in accordance with the present invention is illustrated. The resistor network 10 comprises a substrate 12 comprised of a thermally conductive, electrically insulative material, such as ceramic. In a preferred embodiment of the present invention, an aluminum oxide ceramic is utilized, although other complex oxide ceramics such a stearite, fosterite, porcelain, zirconia, or beryllia may also be advantageously utilized. The substrate 12 has a generally rectangular shape with smooth and flat upper and lower surfaces.

The substrate 12 has a plurality of electrically conductive contact pads 18 provided thereon which provide end terminals for resistive elements 22 of the resistor network. The contact pads 18 also connect to solder balls 24 that provide conductive leads for the resistor network 10. The

resistive elements 22 extend across the lower surface of the substrate 12 between pairs of the contact pads 18 (as shown in phantom in Fig. 2). In such an embodiment, a plurality of isolated resistors are formed in the resistor network 10. Alternatively, the resistive elements 22 may be arranged such that all resistive elements couple to one of the contact pads 18. The resistive elements 22 are covered by a glaze layer 14 that protects and seals the resistive elements, as best illustrated in Fig. 4. Following application of the glaze layer 15, the resistive elements 22 are laser trimmed to the desired values, as discussed below. In turn, the glaze layer 14 is covered by an epoxy layer 16 that protects and seals the laser trimmed resistive elements 22 within the resistor network 10. Finally, the solder balls 24 are electrically coupled to the contact pads 18.

As known in the art, the contact pads 18 and resistive elements 22 are applied to the substrate 12 using a silkscreening process. The contact pads 18 and resistive elements 22 are each provided in the form of a paste that is applied using a mechanized precision stenciling process using screens of stainless steel or nylon. The paste is forced through the screen by a hard rubber squeegee. The shape of the contact pads 18 and the resistive elements 22 is controlled by small openings in the fine mesh screen that correspond to the desired pattern. The pattern of the screen openings is produced by a photographic process from a large scale art work master.

To provide the contact pads 18, a conductive precious metal paste, such as palladium-silver, is applied to the substrate 12, after which the substrate is fired at a temperature of approximately 850°C. to remove all the solvent and binder. The paste that provides the resistive elements 22 is generally comprised of finely powdered inorganic solids (e.g., metals and metal oxides) mixed with a powdered glass binder (e.g., glass frit) and suspended in an organic vehicle

(e.g., a resin mixture). The metal materials for the resistive elements 22 may include silver, palladium, platinum, ruthenium, rhodium and/or gold. Printing and firing of the resistive elements 22 is preferably performed in a humidity and temperature controlled environment. For example, a controlled temperature kiln with various temperature zones between 800°C. and 1200°C. may be used to burn off the organic vehicle and cause a fusion of the glass particles with the ceramic substrate 12. The metallic particles provide a resistive film which is bonded to the substrate 12 as the resistive elements 22. Alternatively, the conductive pads 18 and resistive elements 22 may be fired simultaneously.

Following the application of the resistive elements 22, the glaze layer 14 is printed and fired over the resistive elements as a protective layer. At this time, the resistive elements 22 may also be precision trimmed by laser in order to accurately provide desired resistance values. In this process, portions of the resistive elements 22 are burned away by a laser while monitoring a resistance value of the resistive elements. Next, the epoxy layer 16 is printed and cured over the glaze layer 14 to seal the resistive elements 22 within the resistor array 10. Finally, solder paste is stencilled onto the contact pads 18 and reflowed to form the solder balls 24 that provide the electrically conductive pins of the BGA package. The upper surface of the substrate 12 may also be provided with an epoxy layer. This upper surface can subsequently be printed with graphical or textual information, such as the component, batch or lot identification numbers.

The completed resistor network 10 attaches to a printed circuit board in a manner conventional for BGA packaging. Particularly, associated lands disposed on the printed circuit board engage with the solder balls 24. Electrical conduction between the lands and the solder balls 24 is achieved by solder reflow techniques to fuse the solder balls to the associated lands. Alternatively, a compression bond could be

formed between the solder balls 24 and the lands. The height of the solder balls 24 ensures an adequate gap between the lower surface of the BGA package and the printed circuit board. The ceramic substrate 12 provides good thermal distribution, and allows for the attachment of an additional heat sink as desired. As a result, the resistor network 10 within the BGA package provides good temperature coefficient extension to the printed circuit board.

While the exemplary resistor network 10 of Figs. 2 through 4 provides four isolated resistors, it should be apparent that the teachings of the present invention are applicable to construct a device having any number of isolated or networked resistors. Moreover, the solder balls 24 can be arranged in any type of grid or array format depending on commercial requirements. The resistor network 10 represents a significant improvement over the leadless resistor network 30 since it provides a more compact structure, is easier to manufacture, and provides better thermal capacity. Accordingly, the resistor network 10 could be advantageously utilized in applications requiring device miniaturization, such as in portable or lightweight equipment.

Having thus described a preferred embodiment of a resistor network disposed in a ball grid array package, it should be apparent to those skilled in the art that certain advantages of the within system have been achieved. It should also be appreciated that various modifications, adaptations, and alternative embodiments thereof may be made within the scope and spirit of the present invention. The invention is further defined by the following claims.

CLAIMS

What is Claimed is:

1. A resistor network, comprising:

a substrate having a plurality of electrically conductive pads provided thereon;

at least one resistive element disposed on said substrate interconnecting selected ones of said conductive pads;

a protective layer covering said resistive elements and at least a portion of said substrate; and

a plurality of solder balls respectively coupled to said plurality of conductive pads.

2. The resistor network of Claim 1, wherein said protective layer further comprises a glaze layer covering said resistive elements.

3. The resistor network of Claim 2, wherein said protective layer further comprises an epoxy layer covering said glaze layer.

4. The resistor network of Claim 1, wherein said substrate is comprised of aluminum oxide.

5. The resistor network of Claim 1, wherein said at least one resistive element is disposed on a common surface of said substrate as said solder balls.

6. The resistor network of Claim 1, wherein said at least one resistive element further comprises a plurality of resistive elements interconnecting respective pairs of said conductive pads to provide isolated resistors.

7. The resistor network of Claim 1, wherein said at least one resistive element further comprises a plurality of resistive elements coupled to a common one of said conductive pads.

8. The resistor network of Claim 1, wherein said at least one resistive element are comprised of a material selected from a group including silver, palladium, platinum, ruthenium, rhodium and gold.

9. The resistor network of Claim 1, wherein said solder balls are disposed in an array pattern.

10. A method for making a resistor network in a ball grid array package, the method comprising the steps of:

providing a substrate layer;

printing a plurality of electrically conductive pads onto said substrate layer;

printing resistive material onto said substrate layer interconnecting selected ones of said conductive terminals;

covering said printed resistive material with a protective layer; and

forming a plurality of solder balls respectively onto said plurality of conductive pads.

11. The method of Claim 10, further comprising the step of trimming said printed resistive material to provide a desired resistance value.

12. The method of Claim 10, wherein said step of covering said resistive material further comprises printing and curing a glaze layer covering said resistive material.

13. The method of Claim 12, wherein said step of

covering said resistive material further comprises printing and curing an epoxy layer covering said glaze layer.

14. The method of Claim 10, wherein said substrate layer is comprised of aluminum oxide material.

15. The method of Claim 10, wherein said step of printing resistive material further comprises printing said resistive material on a common surface of said substrate layer on which said solder balls are formed.

16. The method of Claim 10, wherein said step of printing resistive material further comprises interconnecting pairs of said conductive pads with said resistive material to provide isolated resistors.

17. The method of Claim 10, wherein said step of printing resistive material further comprises interconnecting a common one of said conductive pads with said resistive material.

18. The method of Claim 10, wherein said resistive material is comprised of a material selected from a group including silver, palladium, platinum, ruthenium, rhodium and gold.

19. The method of Claim 10, wherein said step of forming a plurality of solder balls further comprises disposing said solder balls in an array pattern.

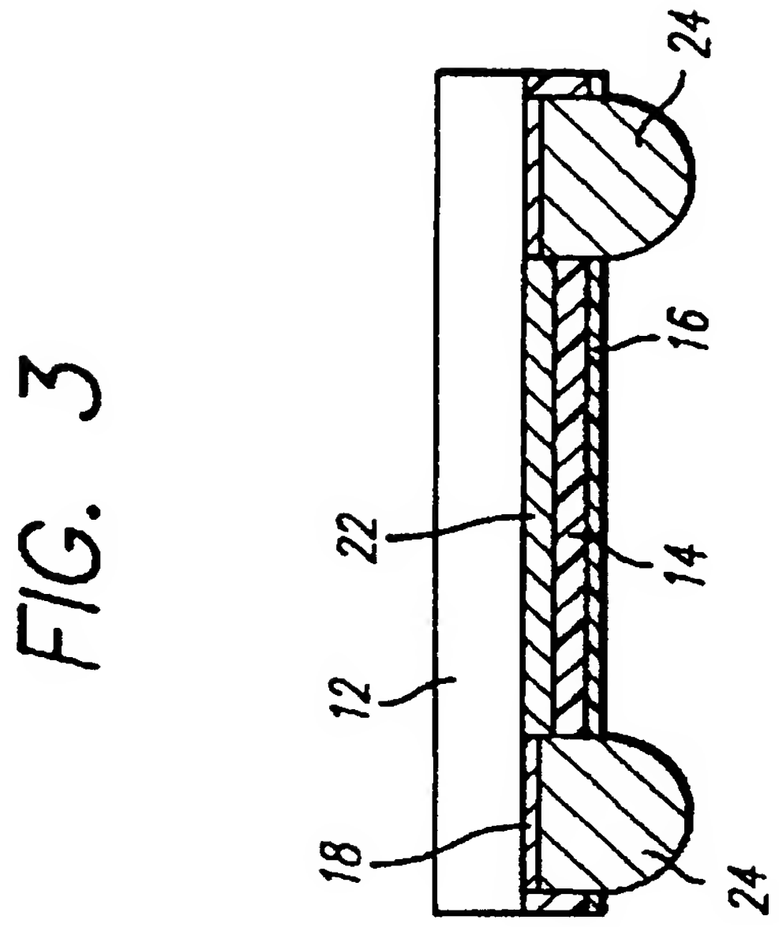

FIG. 3

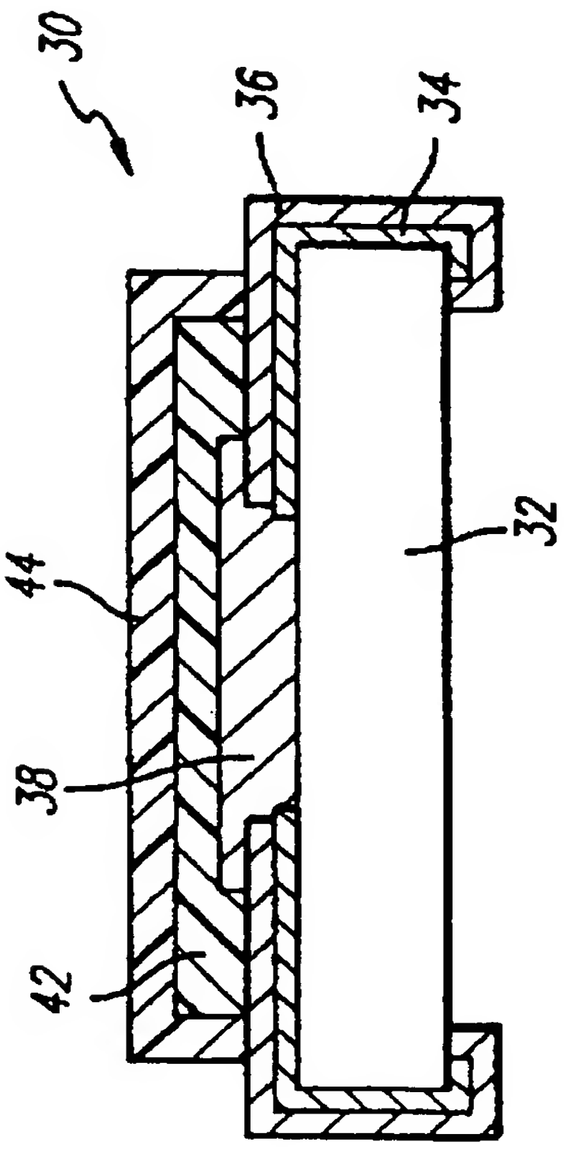

FIG. 1 PRIOR ART

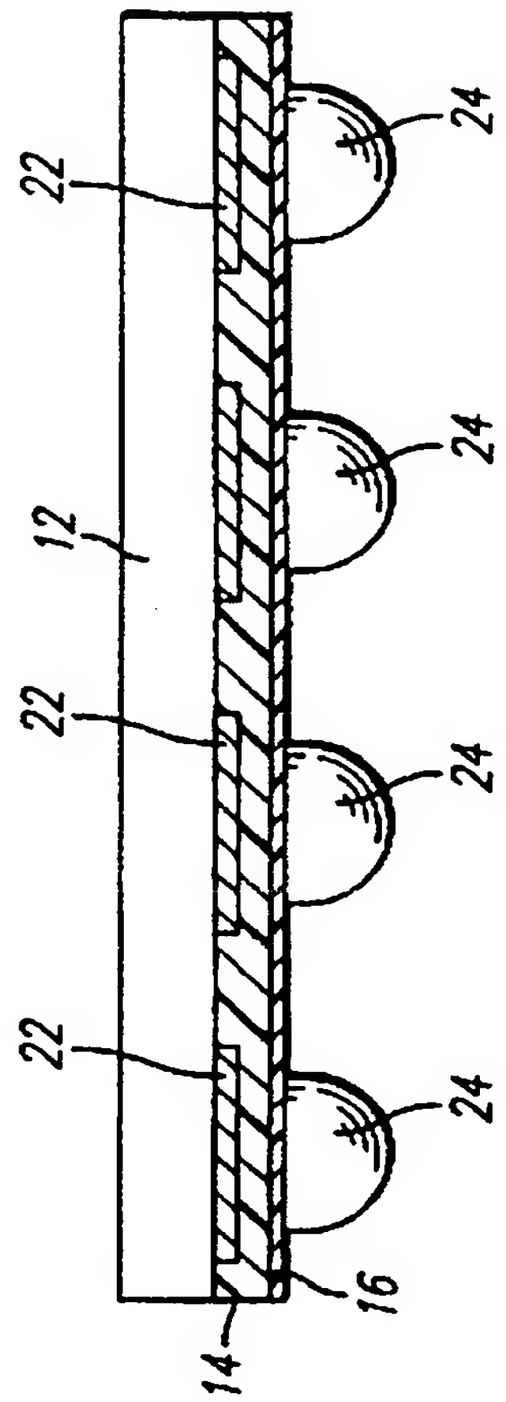

FIG. 4

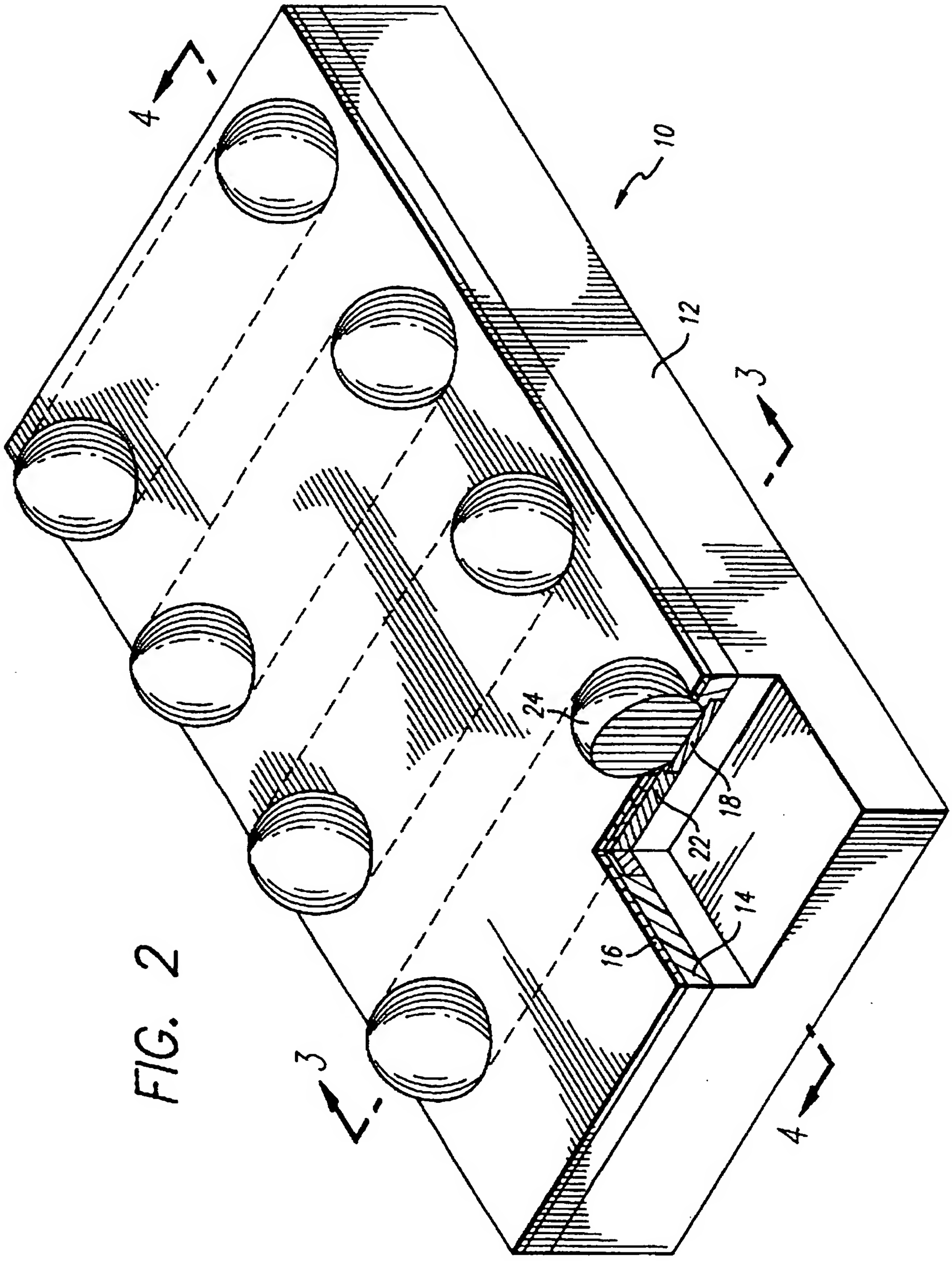

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/01752

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :IPC(6): H01C 1/012
US CL : 338/302
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : 338/302

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 3,909,680 A (TSUNASHIMA) 30 September 1975, col. 2, lines 30-38	8,18
Y	US 4,899,126 A (YAMADA) 06 February 1990, cols. 2-3, lines 65-5.	3,13
X --- Y	US 3,849,757 A (KHAMMOUS ET AL) 19 November 1974, fig. 11.	1 , 2 , 4 - 7 , 9 - 12,14-17,19 --- 3,8,13,18
X --- Y	US 3,745,508 a (BRUDER ET AL) 10 July 1973, col. 5, lines 20-25.	1 - 2 , 5 - 6 , 9 - 12,15-16,19 --- 8,18

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y	JP 3-24901 A (NARITA) 21 February 1991, abstract, figs. 1-14	1-2,5-6,9-12,15-16,19 — 3,8,13,18
X — Y	US 5,586,006 A (SEYAMA ET AL) 17 December 1996, see entire document.	1,10 — 3,13

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